

# INTEGRATED CIRCUIT VERIFICATION SCHEME

## ABSTRACT OF THE DISCLOSURE

A method for minimizing compilation time of a test case during development  
5 testing of an integrated circuit is provided. The method initiates with identifying a test  
case. The test case is associated with the tasks and the tasks are written as text files.  
Then, a file associated with the test case is generated. Next, a sequence of the tasks of the  
file is determined. Then, hardware description language (HDL) tasks, associated with the  
tasks of the file according to the sequence, are identified. Next, a simulation of an  
10 integrated circuit is performed through the HDL tasks. A computer readable medium  
having program instructions for minimizing compilation time of a test case during  
development testing of an integrated circuit and a system for testing an integrated circuit  
design are also provided.